CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously presented). A memory circuit, comprising:

a memory cell array including a plurality of memory cells, said memory cell array including a plurality of word lines and a plurality of bit lines for addressing said plurality of memory cells, said memory cells disposed at crossover points of said words lines with said bit lines;

a plurality of write amplifiers for writing to said plurality of memory cells, each one of said plurality of write amplifiers assigned to a group of said plurality of bit lines; and

an address decoding circuit for simultaneously activating a group of said plurality of write amplifiers, depending on a test mode signal, so that said group of said plurality of write amplifiers writes a test datum to a group of said plurality of memory cells via respectively assigned ones of said plurality of bit lines, by masking a part of an address

of the bit lines which is responsible for selection of a y-segment of the memory cell array.

Claim 2 (original). The memory circuit according to claim 1, further comprising:

a plurality of switching devices;

each one of said plurality of write amplifiers connected to assigned ones of said plurality of bit lines via a respective one of said plurality of switching devices in order to write the test datum from an activated one of said plurality of write amplifiers to an addressed memory cell via one of said plurality of bit lines addressed by a write address.

Claim 3 (original). The memory circuit according to claim 2, wherein said address decoding circuit is configured to simultaneously connect one of said plurality of write amplifiers to assigned ones of said plurality of bit lines depending on the test mode signal.

Claim 4 (previously presented). A method for writing data to a memory circuit, which comprises:

providing a memory cell array including a plurality of memory cells;

providing the memory cell array with a plurality of word lines and a plurality of bit lines for addressing the plurality of memory cells, the memory cells being disposed at crossover points of the word lines and the bit lines;

providing a plurality of write amplifiers for writing to the plurality of memory cells, and assigning each one of the plurality of write amplifiers to a group of the plurality of bit lines;

simultaneously activating a group of said plurality of write amplifiers, depending on a test mode signal, so that the group of the plurality of write amplifiers writes a test datum to a group of the plurality of the memory cells via respectively assigned ones of the plurality of bit lines, by masking a part of an address of the bit lines which is responsible for selection of a y-segment of the memory cell array.

Claim 5 (original). The method according to claim 4, which further comprises simultaneously connecting each amplifier in the group of the plurality of write amplifiers to assigned

ones of the plurality of the bit lines for writing the test datum.

Claim 6 (previously presented). The method according to claim 4, wherein the memory circuit has a plurality of switching devices, each one of the plurality of write amplifiers is connected to assigned ones of said plurality of bit lines via a respective one of the plurality of switching devices for writing the test datum from an activated one of the plurality of write amplifiers to an addressed memory cell via one of the plurality of bit lines addressed by a write address, which further comprises:

activating selected ones of the switching devices in dependence on the test mode signal via the address decoding circuit sending activation signals over column selected lines connected, between the address decoding circuit and the switching devices.

Claim 7 (previously presented). A memory circuit, comprising:

a memory cell array including a plurality of memory cells, said memory cell array including a plurality of word lines and a plurality of bit lines for addressing said plurality of memory cells;

a plurality of write amplifiers for writing to said plurality of memory cells, each one of said plurality of write amplifiers assigned to a group of said plurality of bit lines;

an address decoding circuit for simultaneously activating a group of said plurality of write amplifiers, depending on a test mode signal, so that said group of said plurality of write amplifiers writes a test datum to a group of said plurality of memory cells via respectively assigned ones of said plurality of bit lines, by masking a part of an address of the bit lines which is responsible for selection of a y-segment of the memory cell array;

a plurality of switching devices, each one of said plurality of write amplifiers connected to assigned ones of said plurality of bit lines via a respective one of said plurality of switching devices for writing the test datum from an activated one of said plurality of write amplifiers to an addressed memory cell via one of said plurality of bit lines addressed by a write address; and

column select lines connected between said address decoding circuit and said switching devices, said address decoding

circuit activating selected ones of said switching devices in dependence on the test mode signal.

Claim 8 (canceled).